AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Original) A step-up apparatus comprising:

a first level shift circuit for receiving a first clock signal to generate two phase-opposite second clock signals;

a second level shift circuit for receiving said first clock signal to generate two phase-opposite third clock signals;

a charge pump circuit, connected to said first level shift circuit, for stepping up a power supply voltage at a power supply voltage terminal using said second clock signals to generate a positive voltage; and

a polarity inverting circuit, connected to said charge pump circuit and said second level shift circuit, for inverting said positive voltage using said third clock signals to generate a negative voltage whose absolute value is the same as said positive voltage,

a high level of said second clock signals being not higher than said positive voltage,

a low level of said second clock signals being not lower than a voltage at a ground terminal,

a high level of said third clock signals being not higher than said power supply voltage,

a low level of said third clock signals being not lower than said negative voltage.

2. (Original) The step-up apparatus as set forth in claim 1, wherein said first level shift circuit comprises:

first and second cross-coupled load P-channel MOS transistors whose sources receive said positive voltage; and

first and second N-channel drive MOS transistors whose drains are connected to drains of said first and second cross-coupled load P-channel MOS transistors, respectively,

gates of said first and second N-channel drive MOS transistors receiving said first clock signal and its inverted signal, respectively,

the drains of said first and second N-channel drive MOS transistors generating said second clock signals.

3. (Original) The step-up apparatus as set forth in claim 1, wherein said second level shift circuit comprises:

first and second cross-coupled N-channel Load MOS transistors whose sources receive said voltage at said ground terminal; and

third and second P-channel drive MOS transistors whose sources receive said power supply voltage and whose drains are connected to drains of said first and second cross-coupled load N-channel MOS transistors, respectively,

gates of said first and second drive P-channel MOS transistors receiving said first clock signal and its inverted signal, respectively,

the drains of said first and second P-channel drive MOS transistors generating said third clock signals.

4. (Previously Presented) The step-up apparatus as set forth in claim 1, wherein said charge pump circuit comprises:

a first circuit including a first step-up switching element, connected to said power supply voltage terminal, for generating said power supply voltage; and

an i-th (i=2, 3, ..., K) circuit including a charging capacitor, a first charging element connected between said ground terminal and said charging capacitor, a second charging element connected between said charging capacitor and said power supply voltage terminal, and a second step-up switching element connected to said charging capacitor and said second charging element for generating an "i" times said power supply voltage.

5. (Previously Presented) The step-up apparatus as set forth in claim 4, wherein each of said first and second step-up switching elements comprises a P-channel MOS transistor controlled by one of said second clock signals,

said first charging element comprises an N-channel MOS transistor controlled by the one of said second clock signals, and

said second charging element comprises a P-channel MOS transistor controlled by the other of said second clock signals.

6. (Previously Presented) The step-up apparatus as set forth in claim 1, wherein said charge pump circuit steps up said power supply voltage further using said third clock signals, said pump circuit comprising:

a first circuit including a first step-up switching element, connected to said power supply voltage terminal, for generating said power supply voltage; and

an i-th (i=2, 3, ..., K) circuit including a charging capacitor, a first charging element connected between said ground terminal and said charging capacitor, a second charging element connected between said charging capacitor and said power supply voltage terminal, and a second step-up switching element connected to said charging capacitor and said second charging element for generating an "i" times said power supply voltage,

said first step-up switching element comprising a P-channel MOS transistor controlled by one of said third clock signals,

said second charging element of said 2-nd circuit comprising a P-channel MOS transistor controlled by the other of said third clock signals,

said first charging element of said i-th (i= 2, 3, ...) circuit comprising an N-channel MOS transistor controlled by the one of said second clock signals,

said second charging element of said i-th (i= 3, 4, ...) circuit comprising a P-channel MOS transistor controlled by the other of said second clock signals,

said second step-up switching element comprising a P-channel MOS transistor controlled by the other of said second clock signal.

7. (Original) A step-up apparatus comprising:

a first level shift circuit for receiving a clock first signal to generate two phase-opposite second clock signals;

a second level shift circuit for receiving said first clock signal to generate a third clock signal;

a charge pump circuit, connected to said first level shift circuit, for stepping up a power supply voltage at a power supply voltage terminal using said second clock signals to generate a positive voltage; and

a polarity inverting circuit, connected to said charge pump circuit and said second level shift circuit, for inverting said positive voltage using said third clock signal to generate a negative voltage whose absolute value is the same as said positive voltage,

a high level of said second clock signals being not higher than said positive voltage,

a low level of said second clock signals being not lower than a voltage at a ground terminal,

a high level of said third clock signal being not higher than said voltage at said ground voltage,

a low level of said third clock signal being not lower than said negative voltage.

8. (Original) The step-up apparatus as set forth in claim 7, wherein said first level shift circuit comprises:

first and second cross-coupled load P-channel MOS transistors whose sources receive said positive voltage; and

first and second N-channel drive MOS transistors whose drains are connected to drains of said first and second cross-coupled load P-channel MOS transistors, respectively,

gates of said first and second N-channel drive MOS transistors receiving said first clock signal and its inverted signal, respectively,

the drains of said first and second N-channel drive MOS transistors generating said second clock signals.

9. (Original) The step-up apparatus as set forth in claim 7, wherein said second level shift circuit comprises:

a polarity inverting circuit for inverting said first clock signal;

first and second cross-coupled N-channel Load MOS transistors whose sources receive said negative voltage; and

third and second P-channel drive MOS transistors whose sources receive said voltage at said ground terminal and whose drains are connected to drains of said first and second cross-coupled load N-channel MOS transistors, respectively,

gates of said first and second drive P-channel MOS transistors receiving an output signal of said polarity inverting circuit and its inverted signal, respectively,

the drain of one of said first and second P-channel drive MOS transistors generating said third clock signal.

10. (Original) The step-up apparatus as set forth in claim 9, wherein said polarity inverting circuit comprises a capacitor for receiving said first clock signal and a diode between said capacitor and said ground terminal.

11. (Previously Presented) The step-up apparatus as set forth in claim 7, wherein said charge pump circuit comprises:

a first circuit including a first step-up switching element, connected to said power supply voltage terminal, for generating said power supply voltage; and

an i-th (i=2, 3, ..., K) circuit including a charging capacitor, a first charging element connected between said ground terminal and said charging capacitor, a second charging element connected between said charging capacitor and said power supply voltage terminal, and a second step-up switching element connected to said charging capacitor and said second charging element for generating an "i" times said power supply voltage.

12. (Previously Presented) The step-up apparatus as set forth in claim 11, wherein each of said first and second step-up switching elements comprises a P-channel MOS transistor controlled by one of said second clock signals,

said first charging element comprising an N-channel MOS transistor controlled by the one of said second clock signals,

said second charging element comprising a P-channel MOS transistor controlled by the other of said second clock signals.

13. (Original) A step-up apparatus comprising:

a first level shift circuit for receiving a clock first signal to generate two phase-opposite second clock signals;

a second level shift circuit for receiving said first clock signal to generate two phase-opposite third clock signals;

a charge pump circuit, connected to said first level shift circuit, for stepping up a power supply voltage at a power supply voltage terminal using said second clock signals to generate

first and second positive voltages, said first positive voltage being smaller than said second positive voltage; and

a polarity inverting circuit, connected to said charge pump circuit and said second level shift circuit, for inverting said second positive voltage using said third clock signals to generate a negative voltage whose absolute value is the same as said second positive voltage,

a high level of said second clock signals being not higher than said second positive voltage,

a low level of said second clock signals being not lower than a voltage at a ground terminal,

a high level of said third clock signals being not higher than said power supply voltage,

a low level of said third clock signals being not lower than said negative voltage.

14. (Original) The step-up apparatus as set forth in claim 13, wherein said first level shift circuit comprises:

first and second cross-coupled load P-channel MOS transistors whose sources receive said second positive voltage; and

first and second N-channel drive MOS transistors whose drains are connected to drains of said first and second cross-coupled load P-channel MOS transistors, respectively,

gates of said first and second N-channel drive MOS transistors receiving said first clock signal and its inverted signal, respectively,

the drains of said first and second N-channel drive MOS transistors generating said second clock signals.

15. (Original) The step-up apparatus as set forth in claim 13, wherein said second level shift circuit comprises:

first and second cross-coupled N-channel load MOS transistors whose sources receive said voltage as said ground terminal; and

third and second P-channel drive MOS transistors whose sources receive said power supply voltage and whose drains are connected to drains of said first and second cross-coupled load N-channel MOS transistors, respectively,

gates of said first and second drive P-channel MOS transistors receiving said first clock signal and its inverted signal, respectively,

the drains of said first and second P-channel drive MOS transistors generating said third clock signals.

16. (Previously Presented) The step-up apparatus as set forth in claim 13, wherein said charge pump circuit comprises:

a first circuit including a first step-up switching element, connected to said power supply voltage terminal, for generating said power supply voltage; and

an i-th (i=2, 3, ..., K) circuit including a charging capacitor, a first charging element connected between said ground terminal and said charging capacitor, a second charging element connected between said charging capacitor and said power supply voltage terminal, and a second step-up switching element connected to said charging capacitor and said second charging element for generating an "i" times said power supply voltage,

said L-th (L=2, 3, ..., K-1) circuit generating said first positive voltage,

said K-th (K > L) circuit generating said second positive voltage.

17. (Previously Presented) The step-up apparatus as set forth in claim 16, wherein each of said first and second step-up switching elements comprises a P-channel MOS transistor controlled by one of said second clock signals,

said first charging element comprising an N-channel MOS transistor controlled by the one of said second clock signals,

said second charging element comprising a P-channel MOS transistor controlled by the other of said second clock signals.

18. (Previously Presented) The step-up apparatus as set forth in claim 13, wherein said charge pump circuit steps up said power supply voltage further using said third clock signals, said charge pump circuit further comprising:

a first circuit including a first step-up switching element, connected to said power supply voltage terminal, for generating said power supply voltage; and

an i-th (i=2, 3, ..., K) circuit including a charging capacitor, a first charging element connected between said ground terminal and said charging capacitor, a second charging element connected between said charging capacitor and said power supply voltage terminal, and a second step-up switching element connected to said charging capacitor and said second charging element for generating an "i" times said power supply voltage,

said first step-up switching element comprising a P-channel MOS transistor controlled by one of said third clock signals,

said second charging element of said 2-nd circuit comprising a P-channel MOS transistor controlled by the other of said third clock signals,

said first charging element of said i-th (i= 2, 3, ...,K) circuit comprising an N-channel MOS transistor controlled by the one of said second clock signals,

said second charging element of said i-th (i= 3, 4, ..., K) circuit comprising a P-channel MOS transistor controlled by the other of said second clock signals,

said second step-up switching element comprising a P-channel MOS transistor controlled by the other of said second clock signal,

said L-th (L=2, 3, ..., K-1) circuit generating said first positive voltage,

said K-th (K > L) circuit generating said second positive voltage.

19. (Original) A step-up apparatus comprising:

a first level shift circuit for receiving a clock first signal to generate two phase-opposite second clock signals;

a second level shift circuit for receiving said first clock signal to generate a third clock signal;

a charge pump circuit, connected to said first level shift circuit, for stepping up a power supply voltage at a power supply voltage terminal using said second clock signals to generate first and second positive voltages; and

a polarity inverting circuit, connected to said charge pump circuit and said second level shift circuit, for inverting said second positive voltage using said third clock signal to generate a negative voltage whose absolute value is the same as said second positive voltage,

a high level of said second clock signals being not higher than said second positive voltage,

a low level of said second clock signals being not lower than a voltage at a ground terminal,

a high level of said third clock signal being not higher than said voltage at said ground voltage,

a low level of said third clock signal being not lower than said negative voltage.

20. (Original) The step-up apparatus as set forth in claim 19, wherein said first level shift circuit comprises:

first and second cross-coupled load P-channel MOS transistors whose sources receive said second positive voltage; and

first and second N-channel drive MOS transistors whose drains are connected to drains of said first and second cross-coupled load P-channel MOS transistors, respectively,

gates of said first and second N-channel drive MOS transistors receiving said first clock signal and its inverted signal, respectively,

the drains of said first and second N-channel drive MOS transistors generating said second clock signals.

21. (Original) The step-up apparatus as set forth in claim 19, wherein said second level shift circuit comprises:

a polarity inverting circuit for inverting said first clock signal;

first and second cross-coupled N-channel Load MOS transistors whose sources receive said negative voltage; and

third and second P-channel drive MOS transistors whose sources receive said voltage at said ground terminal and whose drains are connected to drains of said first and second cross-coupled load N-channel MOS transistors, respectively,

gates of said first and second drive P-channel MOS transistors receiving an output signal of said polarity inverting circuit and its inverted signal, respectively,

the drain of one of said first and second P-channel drive MOS transistors generating said third clock signal.

22. (Original) The step-up apparatus as set forth in claim 21, wherein said polarity inverting circuit comprises a capacitor for receiving said first clock signal and a diode between said capacitor and said ground terminal.

23. (Previously Presented) The step-up apparatus as set forth in claim 19, wherein said charge pump circuit comprises:

a first circuit including a first step-up switching element, connected to said power supply voltage terminal, for generating said power supply voltage; and

an i-th (i=2, 3, ..., K) circuit including a charging capacitor, a first charging element connected between said ground terminal and said charging capacitor, a second charging element connected between said charging capacitor and said power supply voltage terminal, and a second step-up switching element connected to said charging capacitor and said second charging switching element for generating an "i" times said power supply voltage,

said L-th (L= 2, 3, ...) circuit generating said first positive voltage,

said K-th (K > L) circuit generating said second positive voltage,

24. (Previously Presented) The step-up apparatus as set forth in claim 23, wherein each of said first and second step-up switching elements comprises a P-channel MOS transistor controlled by one of said second clock signals,

said first charging element comprises an N-channel MOS transistor controlled by the one of said second clock signals, and

said second charging element comprises a P-channel MOS transistor controlled by the other of said second clock signals.

25. (Original) A step-up apparatus comprising:

a first level shift circuit for receiving a clock first signal to generate two phase-opposite second clock signals;

a second level shift circuit for receiving said first clock signal to generate two phase-opposite third clock signals;

a charge pump circuit, connected to said first level shift circuit, for stepping up a power supply voltage at a power supply voltage terminal using said second clock signals to generate first and second positive voltages, said first positive voltage being smaller than said second positive voltage; and

a polarity inverting circuit, connected to said charge pump circuit and said second level shift circuit, for inverting said first positive voltage using said third clock signals to generate a negative voltage whose absolute value is the same as said first positive voltage,

a high level of said second clock signals being not higher than said first positive voltage,

a low level of said second clock signals being not lower than a voltage at a ground terminal,

a high level of said third clock signals being not higher than said power supply voltage,

a low level of said third clock signals being not lower than said negative voltage.

26. (Original) The step-up apparatus as set forth in claim 25, wherein said first level shift circuit comprises:

first and second cross-coupled load P-channel MOS transistors whose sources receive said first positive voltage; and

first and second N-channel drive MOS transistors whose drains are connected to drains of said first and second cross-coupled load P-channel MOS transistors, respectively,

gates of said first and second N-channel drive MOS transistors receiving said first clock signal and its inverted signal, respectively,

the drains of said first and second N-channel drive MOS transistors generating said second clock signals.

27. (Original) The step-up apparatus as set forth in claim 25, wherein said second level shift circuit comprises:

first and second cross-coupled N-channel Load MOS transistors whose sources receive said voltage as said ground terminal; and

third and second P-channel drive MOS transistors whose sources receive said power supply voltage and whose drains are connected to drains of said first and second cross-coupled load N-channel MOS transistors, respectively,

gates of said first and second drive P-channel MOS transistors receiving said first clock signal and its inverted signal, respectively,

the drains of said first and second P-channel drive MOS transistors generating said third clock signals.

28. (Previously Presented) The step-up apparatus as set forth in claim 25, wherein said charge pump circuit comprises:

a first circuit including a first step-up switching element, connected to said power supply voltage terminal, for generating said power supply voltage; and

an i-th (i=2, 3, ..., L) circuit including a charging capacitor, a first charging element connected between said ground terminal and said charging capacitor, a second charging element connected between said charging capacitor and said power supply voltage terminal, and a second step-up switching element connected to said charging capacitor and said second charging element for generating an "i" times said power supply voltage,

a K-th (K=2, 3, ...,L-1) circuit generating said first positive voltage, and

an L-th (L > K) circuit generating said second positive voltage.

29. (Previously Presented) The step-up apparatus as set forth in claim 28, wherein each of said first and second step-up switching elements comprises a P-channel MOS transistor controlled by one of said second clock signals,

said first charging element comprising an N-channel MOS transistor controlled by the one of said second clock signals,

said second charging element comprising a P-channel MOS transistor controlled by the other of said second clock signals.

30. (Previously Presented) The step-up apparatus as set forth in claim 25, wherein said charge pump circuit steps up said power supply voltage further using said third clock signals, said pump circuit comprising:

a first circuit including a first step-up switching element, connected to said power supply voltage terminal, for generating said power supply voltage; and

an i-th (i=2, 3, ..., L) circuit including a charging capacitor, a first charging element connected between said ground terminal and said charging capacitor, a second charging element connected between said charging capacitor and said power supply voltage terminal, and a second step-up switching element connected to said charging capacitor and said second charging element for generating an "i" times said power supply voltage,

said first step-up switching element comprising a P-channel MOS transistor controlled by one of said third clock signals,

said second charging element of said 2-nd circuit comprising a P-channel MOS transistor controlled by the other of said third clock signals,

said first charging element of said i-th (i= 2, 3, ..., L) circuit comprising an N-channel MOS transistor controlled by the one of said second clock signals,

said second charging element of said i-th (i= 3, 4, ..., L) circuit comprising a P-channel MOS transistor controlled by the other of said second clock signals,

said second step-up switching element comprising a P-channel MOS transistor controlled by the other of said second clock signal,

a K-th (K=2, 3, ..., L-1) circuit generating said first positive voltage, and

an L-th (L > K) circuit generating said second positive voltage.

31. (Original) A step-up apparatus comprising:

a first level shift circuit for receiving a clock first signal to generate two phase-opposite second clock signals;

a second level shift circuit for receiving said first clock signal to generate a third clock signal;

a charge pump circuit, connected to said first level shift circuit, for stepping up a power supply voltage at a power supply voltage terminal using said second clock signals to generate first and second positive voltages; and

a polarity inverting circuit, connected to said charge pump circuit and said second level shift circuit, for inverting said first positive voltage using said third clock signal to generate a negative voltage whose absolute value is the same as said first positive voltage,

a high level of said second clock signals being not higher than said first positive voltage,

a low level of said second clock signals being not lower than a voltage at a ground terminal,

a high level of said third clock signal being not higher than said voltage at said ground voltage,

a low level of said third clock signal being not lower than said negative voltage.

32. (Original) The step-up apparatus as set forth in claim 31, wherein said first level shift circuit comprises:

first and second cross-coupled load P-channel MOS transistors whose sources receive said first positive voltage; and

first and second N-channel drive MOS transistors whose drains are connected to drains of said first and second cross-coupled load P-channel MOS transistors, respectively,

gates of said first and second N-channel drive MOS transistors receiving said first clock signal and its inverted signal, respectively,

the drains of said first and second N-channel drive MOS transistors generating said second clock signals.

33. (Original) The step-up apparatus as set forth in claim 31, wherein said second level shift circuit comprises:

a polarity inverting circuit for inverting said first clock signal;

first and second cross-coupled N-channel Load MOS transistors whose sources receive said negative voltage; and

third and second P-channel drive MOS transistors whose sources receive said voltage at said ground terminal and whose drains are connected to drains of said first and second cross-coupled load N-channel MOS transistors, respectively,

gates of said first and second drive P-channel MOS transistors receiving an output signal of said polarity inverting circuit and its inverted signal, respectively,

the drain of one of said first and second P-channel drive MOS transistors generating said third clock signal.

34. (Original) The step-up apparatus as set forth in claim 33, wherein said polarity inverting circuit comprises a capacitor for receiving said first clock signal and a diode between said capacitor and said ground terminal.

35. (Previously Presented) The step-up apparatus as set forth in claim 31, wherein said charge pump circuit comprises:

a first circuit including a first step-up switching element, connected to said power supply voltage terminal, for generating said power supply voltage; and

an i-th (i=2, 3, ..., L) circuit including a charging capacitor, a first charging element connected between said ground terminal and said charging capacitor, a second charging element connected between said charging capacitor and said power supply voltage terminal, and a second step-up switching element connected to said charging capacitor and said second charging element for generating an "i" times said power supply voltage,

a K-th (K= 2, 3, ...) circuit generating said first positive voltage, and

an L-th (L > K) circuit generating said second positive voltage,

36. (Previously Presented) The step-up apparatus as set forth in claim 35, wherein each of said first and second step-up switching elements comprises a P-channel MOS transistor controlled by one of said second clock signals,

said first charging element comprising an N-channel MOS transistor controlled by the one of said second clock signals,

said second charging element comprising a P-channel MOS transistor controlled by the other of said second clock signals.

37. (Previously Presented) A step-up apparatus comprising:

a first level shift circuit for receiving a first clock signal to generate a 2nd clock signal, a 3rd clock signal, ..., a K-th clock signal (K= 2, 3, ...) having a definite voltage swing;

a second level shift circuit for receiving said first clock signal to generate two phase-opposite third clock signals;

a charge pump circuit, connected to said first level shift circuit, for stepping up a power supply voltage at a power supply voltage terminal using said first, second, ..., K-th clock signals to generate a positive voltage; and

a polarity inverting circuit, connected to said charge pump circuit and said second level shift circuit, for inverting said positive voltage using said third clock signals to generate a negative voltage whose absolute value is the same as said positive voltage.

38. (Previously Presented) The step-up apparatus as set forth in claim 37, wherein said charge pump circuit comprises:

a first circuit including a first step-up switching element, connected to said power supply voltage terminal, for generating said power supply voltage in accordance with said first clock signal;

an i-th (i=2, 3, ..., K) circuit including a charging capacitor, a first charging element connected between said ground terminal and said charging capacitor, a second charging element connected between said charging capacitor and said power supply voltage terminal, and a second step-up switching element connected to said charging capacitor and said second charging element for generating an "i" times said power supply voltage.

39. (previously presented): The step-up apparatus as set forth in claim 38, wherein said first step-up switching element comprises a P-channel MOS transistor controlled by said first clock signal,

said first charging element comprising an N-channel MOS transistor controlled by said first clock signal,

said second charging element comprising an N-channel MOS transistor controlled by said second clock signal,

said second step-up switching element of said i-th (i= 2, 3, ..., K) circuit comprising a P-channel MOS transistor controlled by said i-th clock signal.

40. (Original) The step-up apparatus as set forth in claim 38, wherein said first level shift circuit comprises an i-th (i= 2, 3, ..., K) level shift unit is powered by (i-2) $\cdot V_{DD}$, (i-1) $\cdot V_{DD}$ and i-V_{DD} where V_{DD} is a power supply voltage.

41. (Original) The step-up apparatus as set forth in claim 40, wherein said i-th level shift unit comprises:

cross-coupled first and second load N-channel MOS transistors whose sources receive $(i-2) \cdot V_{DD}$;

first and second drive P-channel MOS transistors whose sources receive $(i-1) \cdot V_{DD}$ and whose drains are connected to drains of said first and second load N-channel MOS transistors, respectively;

cross-coupled first and second load P-channel MOS transistors whose sources receive $i \cdot V_{DD}$; and

first and second drive N-channel MOS transistors whose sources receive $(i-2) \cdot V_{DD}$, whose drains are connected to drains of said first and second load P-channel MOS transistors, respectively, and whose gates are connected to gates of said first and second load N-channel MOS transistors, respectively,

gates of said first and drive P-channel MOS transistors receiving said (i-1)-th clock signal and its inverted signal,

the drain of said second drive N-channel MOS transistor generating said i-th clock signal via an inverter.

42. (Canceled)

43. (Canceled)

44. (Currently Amended) A step-up apparatus comprising:

a level shift circuit for receiving a first clock signal to generate a 2nd clock signal, a 3rd clock signal, ..., a K-th clock signal (K= 2, 3, ...) having a definite voltage swing; and

a charge pump circuit, connected to a first level shift circuit, for stepping up a power supply voltage at a power supply voltage terminal using said first, second, ..., K-th clock signals to generate a positive voltage, said charge pump comprising:

a first circuit including a first step-up switching element, connected to said power supply voltage terminal, for generating said power supply voltage in accordance with said first clock signal;

an i-th (i=2, 3, ..., K) circuit including a charging capacitor, a first charging element connected between a ground terminal and said charging capacitor, a second charging element connected between said charging capacitor and said power supply voltage terminal, and a second step-up switching element connected to said charging capacitor and said second charging element for generating an "i" times said power supply voltage, wherein

said second step-up switching element of said i-th (i= 2, 3, ..., K) circuit comprises a P-channel MOS transistor controlled by an i-th clock signal,

~~The step-up apparatus as set forth in claim 42,~~ wherein:

said first step-up switching element comprises a P-channel MOS transistor controlled by said first clock signal,

said first charging element comprising an N-channel MOS transistor controlled by said first clock signal, and

said second charging element comprising an N-channel MOS transistor controlled by said second clock signal.

45. (Currently Amended) A step-up apparatus comprising:

a level shift circuit for receiving a first clock signal to generate a 2nd clock signal, a 3rd clock signal, ..., a K-th clock signal (K= 2, 3, ...) having a definite voltage swing; and

a charge pump circuit, connected to a first level shift circuit, for stepping up a power supply voltage at a power supply voltage terminal using said first, second, ..., K-th clock signals to generate a positive voltage, said charge pump comprising:

a first circuit including a first step-up switching element, connected to said power supply voltage terminal, for generating said power supply voltage in accordance with said first clock signal;

an i-th (i=2, 3, ..., K) circuit including a charging capacitor, a first charging element connected between a ground terminal and said charging capacitor, a second charging element connected between said charging capacitor and said power supply voltage terminal, and a second step-up switching element connected to said charging capacitor and said second charging element for generating an "i" times said power supply voltage, wherein

said second step-up switching element of said i-th (i= 2, 3, ..., K) circuit comprises a P-channel MOS transistor controlled by an i-th clock signal,

~~The step-up apparatus as set forth in claim 42,~~

wherein said level shift circuit comprises an i-th (i= 2, 3, ..., K) level shift unit is powered by (i-2) · V_{DD}, (i-1) · V_{DD} and i-V_{DD} where V_{DD} is a power supply voltage.

46. (Currently Amended) A step-up apparatus comprising:

a level shift circuit for receiving a first clock signal to generate a 2nd clock signal, a 3rd clock signal, ..., a K-th clock signal (K= 2, 3, ...) having a definite voltage swing; and

a charge pump circuit, connected to a first level shift circuit, for stepping up a power supply voltage at a power supply voltage terminal using said first, second, ..., K-th clock signals to generate a positive voltage, said charge pump comprising:

a first circuit including a first step-up switching element, connected to said power supply voltage terminal, for generating said power supply voltage in accordance with said first clock signal;

an i-th (i=2, 3, ..., K) circuit including a charging capacitor, a first charging element connected between a ground terminal and said charging capacitor, a second charging element connected between said charging capacitor and said power supply voltage terminal, and a second step-up switching element connected to said charging capacitor and said second charging element for generating an "i" times said power supply voltage, wherein

said second step-up switching element of said i-th (i= 2, 3, ..., K) circuit comprises a P-channel MOS transistor controlled by an i-th clock signal,

~~The step-up apparatus as set forth in claim 42, wherein:~~

wherein said i-th level shift unit comprises:

cross-coupled first and second load N-channel MOS transistors whose sources receive $(i-2) \cdot V_{DD}$;

first and second drive P-channel MOS transistors whose sources receive $(i-1) \cdot V_{DD}$ and whose drains are connected to drains of said first and second load N-channel MOS transistors, respectively;

cross-coupled first and second load P-channel MOS transistors whose sources receive $i \cdot V_{DD}$; and

first and second drive N-channel MOS transistors whose sources receive $(i-2) \cdot V_{DD}$, whose drains are connected to drains of said first and second load P-channel MOS transistors, respectively, and whose gates are connected to gates of said first and second load N-channel MOS transistors, respectively,

gates of said first and drive P-channel MOS transistors receiving an (i-1)-th clock signal and its inverted signal,

the drain of said second drive N-channel MOS transistor generating said i-th clock signal via an inverter.

47. (Canceled)